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Implementation of Reconfigurable Router Architecture for NoC

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ABSTRACT

Network on chip (NoC) becomes a promising solution for intercommunication infrastructure in System on Chip (SoC) as traditional methods exhibit severe bottlenecks at intercommunication among processor elements. However, designing of NoC is majorly complex because of lot of issues raise in terms of performance metrics such as system scalability, latency, power consumption and signal integrity. This paper discussed issues of memory unit in router and thereafter, proposing advanced memory structure. To obtain efficient data transfer, FIFO buffers are implemented in distributed RAM and virtual channels for FPGA based NoC. An advanced FIFO based memory units are proposed in NoC router and the performance is evaluated in Bi-directional NoC (Bi-NoC). The major motivation of this paper is to reduce burden of router while improving FIFO internal structure. To enhance the speed data transfer, Bi-NoC with a self-configurable intercommunication channel is proposed. The Simulations and synthesis results are proven guaranteed throughput, predictable latency, and fair network access highly provided when compared to recent works.

KEYWORDS: Bi-NoC; FIFO; Virtual Channel; Switch Allocator; Router; SoC.

1.INTRODUCTION

Field-programmable gate array (FPGA) is one of fastest growing industries to provide high performance to real-time applications. However, the size and loss in yield are increasing with decreasing of channel length of CMOS. Moore proposed that the number of devices in system is double at every Eighteen months therefore concentrating on different aspects while designing of application based on VLSI technology. To accommodate higher operating frequencies with the increasing transistor density, and shorter time-to-market pressure, chip multiprocessor (CMP) and multiprocessor system on chip (MPSoC) architectures are proposed. The bus structures for on-chip communication and combined complex heterogeneous functional devices on a single chip are more and more required in today's semiconductor industry. The traditional intercommunication architectures are unable to

provide huge performance in case of MPSoC and CMP. Network-on- chip (NoC) is one of popular solutions for the problems of intercommunication among processing Elements (PEs) in systems-on-chip (SoC). Using NoC as tool for intercommunication for FPGAs is not a new idea, whereas the existed interconnecting methods like crossbars exhibit poor scalability therefore the development of new NoC architectures are the best suited to FPGA. Designing of new NoC architecture is still a challenging problem for researchers to achieve high performance without sacrifice of speed and throughput. NoC is the term mentioned to explain an intercommunication architecture that is maintaining of design solutions for communication-centric trends. A typical NoC architecture consists of multiple segments of wires and various routers to transfer the data among PEs. In the Tile based architecture, NoC is framed like city-block style which configures the wires and routers like a street grids and PEs are separated by wires that are placed on city blocks. Apart from routers and PEs, Network Interface (NI) is one of important design constraint for NoC because it transforms data packet PEs into fixed length of flow control digits (flits). The entire data packet is mainly divided into three flits that are header, body and tail flit. Theses flits are forwarded and routed with control mechanisms towards the destination through current router to neighbor router. In the city-block based tile NoC, router is composed with five bi-directional input and output ports that are east, south, west, north and local port of associated PE. To intercommunicate between the ports efficiently, each bi-directional port is connected neighbor port with set of physical interconnected wires. The router is known as the heart of NoC because it transfers and controls the data based on various methodologies. To describe the function of router, a 5X5 crossbar switch presented. The crossbar switch moves the data from the selected input port to output port based on control logic. An arbiter is required to select Appropriate input port to transfer data depending on priority among the input ports. Hence, typical NoC router consists of five input and out ports, crossbar switch and arbiter modules to intercommunicated PEs. Fig.1 described the structure of 3X3 mesh based NoC where center router consists of 5X5 bi- directional ports. Source Intellectual Property (IP) initiates the data packet transferring through NI and current router receives thereafter transfers to neighbour router which is located towards destination IP. The routing of data packet from source to destination depends on the routing algorithm which is integrated in each router. In typical NoC, X-Y deterministic routing algorithm that routes the data based on X and Y coordinates is used to transfer from source to destination. Topology is one of the major constraints for routing algorithm because measuring distance of source to destination router is quite complex in case of routers not aligned properly. Most of the routing algorithms are used mesh topology as it is simple to implement. Fig.1 clearly describes X-Y routing algorithm in mesh topology from source to destination. Source IP measures the Distance of destination in terms of number of router and locks the path until data packet reaches to destination. The address of destination and information of intermediated routers are added to the data packet before starting data packet transfer. This paper identifies the limitations of memory based NoC and considers to devices that require enough to contain SoC. The size of an FPGA is evaluated in Logic Cells (LCs) which are equivalent to a four-input Lookup Table (LUT).

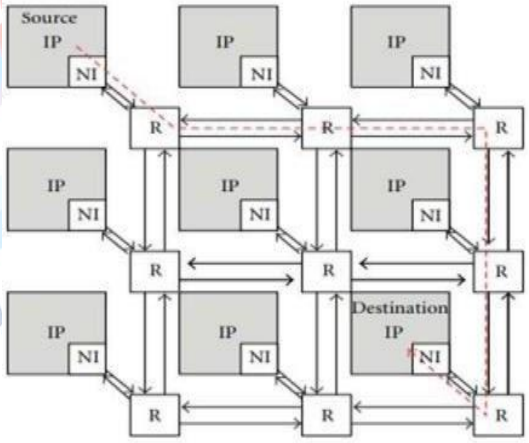


Fig.1: 3X3 mesh based NoC architecture

2. RELATED WORK

The on-chip interconnected network is proposed for general purpose of intercommunication among PEs instead of on-chip wires. The PEs are connected to on-chip network in place of dedicated wires therefore data packets are routed among them. The On- chip network utilizes global wires thereby optimizing electrical properties and properly maintained. The controlled electrical wires present low crosstalk properties and less power consumption by maintaining signal and occupies a little area on chip. W. J. Dally and

B. Towles conclude the paper with different research directions of on-chip such as NI, topologies and flow control methods. Sunetal proposed structure of dynamic router which is unbalance traffic. The advanced router composed inter and intra port buffer mechanism that creates efficient utilization of buffer resources and avoids the head-of-line blocking error. This proposed router is solving of unbalanced traffic problem effectively between current router and neighbor router. The simulation results presented balance traffic among ports and also increased buffer utilization by paired with a Flip-Flop (FF). A memory Controller is a common module of SoC that requires several thousands of LCs.FPGA producers and proposed a RingNet based memory oriented NoC. Because of distinctive feature, the RingNet based memory oriented NoC uses intercommunication through Centrally located memory which prevents network congestions and also requires buffer therefore efficient utilization of FPGA resources. Network buffer is structured with distributed RAM and efficient switching technique of virtual cut- through (VCT) used to obtain guaranteed throughput, network access and predictable latency. The FPGA is optimized by 3-port switches that are organized into ladder of tree topology and small memory in switches such as distributed memory and VCT based data switching. Hence, RingNet based NoC presents improved maximum clock frequency and also resource consumption. However, power consumption is drawback when Ring Net based NoC used in complex SoC. By directions from recent work, this paper proposing an advanced FIFO buffer proposed which is compatible to virtual channel buffered strategy. To improve the data transfer speed, Bi- directional NoC is utilized as it has a distinctive feature of self-reconfigurable. By presenting Bi-NoC with advanced FIFO buffer, this paper presents enhanced maximum clock frequency, memory utilization.

3. ADVANCED NOC DESIGN

This section of paper describes the structure of NoC router composed with advanced FIFO buffer and Bi-NoC with self-reconfigurable channels. Initially flow control mechanism discussed and then followed by structure of advanced router. This paper composed with buffered strategy for data flow control mechanism because of buffer decouples channel allocation thereby improving the efficiency of flow control of whereas in buffered-less strategy, the data packet misrouted or dropped if two channels are allocated a single packet. The buffered flow can be classified into two types that are packet flow and flite flow and again packet and flite flow control divided into two types. The store and forward and virtual cut through are belongs to packet flow whereas Wormhole and virtual channel belongs to flite flow control mechanism. Fig.2 shows typical structure of Bi- NoC such as Bi-NoC router consists of three stages of data control that are Routing Computation (RC), Switch Allocator (SA) and Switch Traversal (ST). RC module generates and sends the channel request to SA to transfer data on each buffer. The SA Acknowledges same based on availability in FIFO buffer. SA allocates the channel and transfers data to ST stage whenever vacant space available in buffer of neighbor router. In ST stage, the data flits are transferred from input to output port through crossbar switch. To avoid head of line (HoL) error, virtual channel based data switching is proposed that composes buffer and protects the data flites. In virtual flow control, virtual channel is assigned to data flite whenever entire data flites are not reached neighbor router. When head flite reaches to queue of buffer through virtual channel therefore it moves to RC stage which decodes and routes request towards associated direction. The FIFO of conventional router at center and traffic increased huge because of next flite must wiat until current flite transferred to neighbor router.

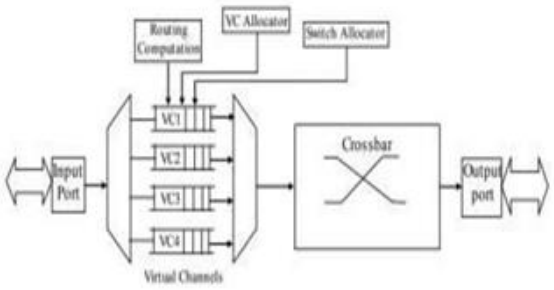


Fig.2 Typical structure of Bi-NoC

To address this issue, the proposed work distributes the FIFO structure into different stages and also physical channel is divided number of virtual channels. Hence next flite waiting period is reduced and data transfer speed is increased.

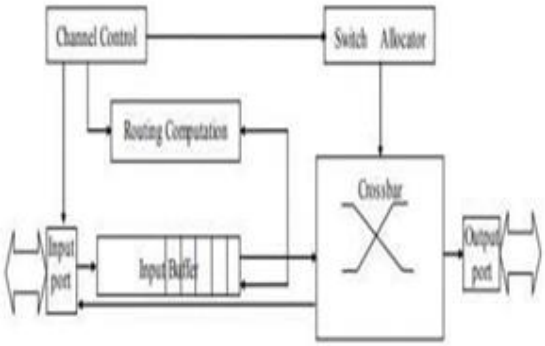


Fig.3 Structure of Bi- NoC with virtual channel allocation

The direction of request transfers to the virtual channel allocation (VA) stage to select associated virtual channel of neighbor router. Because number of requests to access same virtual channel, there may be contention will occur among data flites. The flites which are accessed virtual channel should be present in the current router as previous router is blocked due to contention. Once data flites crosses the VA stage, it assigns to SA stage that presents physical channel into neighbor router. By multiplexing virtual channels to buffer, free data packets never block other data packets which are ready transferred to the Destination trough physical channel. Fig.3 describes the data transfer with help of virtual channels when physical channel is busy or blocked in Bi- NoC .This structure enables multiple virtual channels with physical channel of associated buffer thereby increasing throughput and avoiding deadlock error. The flow of virtual channel in router from input port to output port is as shown Fig.3. The incoming flit which has high priority arrives to the neighbor router accessed appropriate virtual channel initially; thereafter entire data packet will be processed. The incoming first flit of data packet is head flit which arrives to top of virtual channel queue of the buffer thereby entering into RC stage. It decodes in RC stage and creates respective direction of request towards destination router. The direction request of flit transfers to VA stage to obtain selected virtual channels towards destination router.

4. EXISTING METHOD

In existing method the structure of NoC router is designed with advanced FIFO buffer and Bi- NoC with self- reconfigurable channels. Initially flow control mechanism discussed and then followed by structure of advanced router. This paper composed with buffered strategy for data flow control mechanism because of buffer decouples channel allocation thereby improving the efficiency of flow control whereas in buffered-less strategy, the data packet misrouted or dropped if two channels are allocated a single packet. The buffered flow is classified into two types that are packet flow and flite flow and again packet and flite flow control divided into two types. The store and forward and virtual cut through are belongs to packet flow whereas Wormhole and virtual channel belongs to flite flow control mechanism.

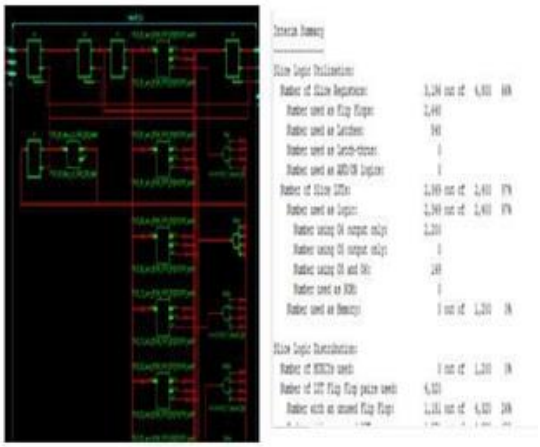


Fig. 4 RTL SCHEMATIC DAIGRAM

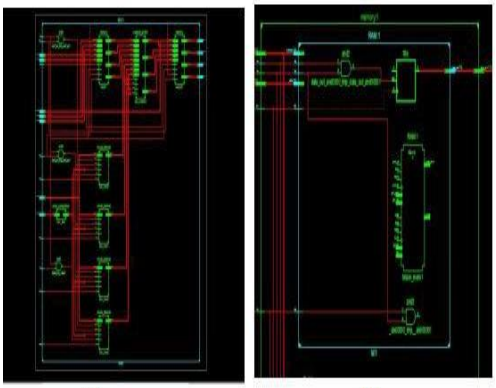
DISADVANTAGES

- Complex FIFO memory is required for queuing the incoming packets
- Very poor energy efficiency.

5. PROPOSED METHOD

An advanced FIFO structure based NoC is simulated and synthesized in Xilinx 14.5 ISE and implemented Vertex-6 FPGA device to analyze the performance in terms of occupied area, latency, power consumption and throughput. Single router is designed initially and then designed mesh based NoC to realize the memory utilization of FPGA. Fig.4 indicates that Register Transfer Level (RTL) schematic of single NoC router which is composed with input and output ports, arbiter, crossbar and channel control modules. The figure also describes the utilizations in terms of memory units each component individually. Each module of NoC designed using Verilog Hardware Description Language (HDL) separately and integrated as one module. An advanced queued buffer is designed both typical NoC and Bi- directional NoC thereby comparing both

designs easily. The simulation results are analyzed area utilization in terms of occupied number of slices registers, LUT-FF pairs and slice registers), latency in terms of delay, Maximum operating frequency, power consumption in terms of dynamic power dissipation, memory utilization in terms of number of RAMs, and finally, throughput in terms of flits per sec., node.



[A] [B]

Fig.4.1 RTL level schematic diagrams of Bi-NoC

6. RESULTS

Table1 clearly shows the comparison of Ring Net and advanced Bi-NoC in terms of Efficient resource utilization. The resource utilization represented in terms of occupied LUTs and FFs which is extremely less when it is compared with Ring Net. Table inferences clearly memory utilization of advanced Bi-NoC is requiring comparatively less because of sharing queued buffer between neighbor routers and data transferred in terms of flits.

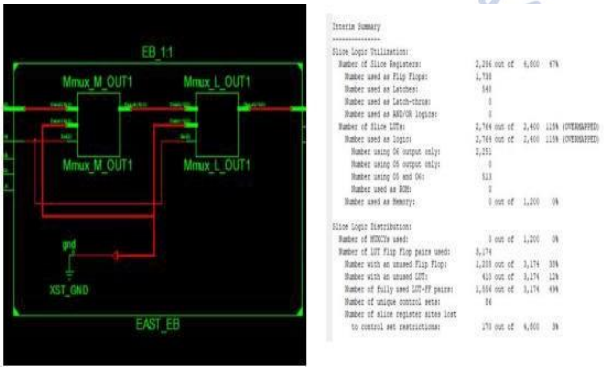


Fig.5 RTL level schematic diagrams of Bi-NoC

TABLE 1: Comparison of existing and proposal

Architecture	Resources Utilized		Delay (ns)
	LUTs	FFs	
RingNet [15]	497	884	0.712
Bi-NoC	327	728	0.511

7. CONCLUSION

The solution for intercommunication of SoC such as parallel communication wires and also removes barriers of bus based communication. In this paper, an advanced memory unit is proposed and implemented in Bi-NoC to achieve less memory requirement of buffer and also high-performance in terms of Maximum operating bandwidth. When compared to previous work, the proposed work improved approximately 28% delay and 17% resources utilization. As Ring Net used Round robin arbiter, the resources utilization is more than proposed work. Data packet divided into number of flits and queued buffer is shared between neighbor routers thereby requiring of buffer size is less when data transferred through data flits from source to destination. This advanced router design integrated in Bi-NoC configuration to achieve higher data transfer speed when compared to typical NoC. Virtual channels are created between routers when data flit is block in case of physical channel is not available therefore data packet latency is reduced as well as deadlock error avoided. The implementation results are improved in terms of resource utilization when compared with existing work. In future, NoC based processors are used at Artificial Intelligence applications. The performance NoC is needed to be improved by advancing router components because the power consumption increased through virtual channels at advanced FIFO structure

Conflict of interest statement

Authors declare that they do not have any conflict of interest.

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